REMARKS

Claims 51-81 remain in the application. Claim 79-81 are newly added, but do not add any new matter.

The present invention relates to the use of certain set-up pulses to increase contrast and drive time to produce higher quality images on a plasma display panel. (Pg. 5, lns. 26-27) Set-up pulses are used to prime the Plasma Display Panel (PDP) cells to ensure a proper discharge and to improve contrast and light efficiency. As PDPs become larger in size with more cells while high definition cells becoming smaller, power, heat, and light issues become more critical. For example, high definition PDPs may have resolutions of 1920 x 1080 pixels. (Pg. 1, lns. 24 – 26). Since refresh rates can be regulated or standardized, the refresh rate may remain constant or actually increase as technology improves. Thus, more cells may need to be primed in the same amount of time period. However, priming more cells in the same amount of time period means that there is less time to prime each cell. Thus, improper discharges could occur and contrast may deteriorate. The present invention addresses the problem of these new demands by providing an appropriate priming of the cells and also shortening of the time require for the set-up period.

The Office Action rejected Claims 51-78 as being unpatentable over Applicant's Admitted Prior Art (hereinafter "AAPA") in view of *Yamamoto et al.* (U.S. 5,142,200, hereinafter "*Yamamoto*").

The Office Action admits that AAPA does not disclose "wherein the set-up pulse applied in the set-up step has a waveform that rises at an average voltage change rate of no greater than 6 V/μs, and that starts to fall at a rate greater than the average voltage change rate at a time period of the rising."

Furthermore, *Yamamoto* does not teach or suggest "wherein the set-up pulse applied in the set-up step has a waveform that rises at an average voltage change rate of no greater than 6 V/μs, and that starts to fall at a rate greater than the average voltage change rate at a time period of the rising." The Office Action cited *Yamamoto* for teaching the use of a 20 to 150 μs rise time to substantially reach the driving voltage of 150 volts (Col. 5, lns. 24 – Col. 6, lns 2). *Yamamoto* teaches alterations to the sustain pulse. (Col. 1, lns. 15-16). The sustain pulse, however, is different from the set-up pulse. As disclosed above, the set-up pulse is applied to the scan electrodes 19a to set-up the discharge cells. The sustain pulse is applied across the scan electrodes and the sustain electrodes 19b, causing the discharge cells to discharge the wall charge that has accumulated. (Spec, Pg. 4, lns. 5-15).

Furthermore, *Yamamoto* does not teach a 20 to 150 μs rise time, but rather a 20 to 150 ns rise time. With a 20 – 150 ns rise time, the pulse rises at 1 V/ns to 7.5 V/ns, which is equivalent to 1000 V/μs to 7500 V/μs. A 1000 V/μs to 7500 V/μs rise rate is well beyond the 6 V/μs disclosed in the current claims.

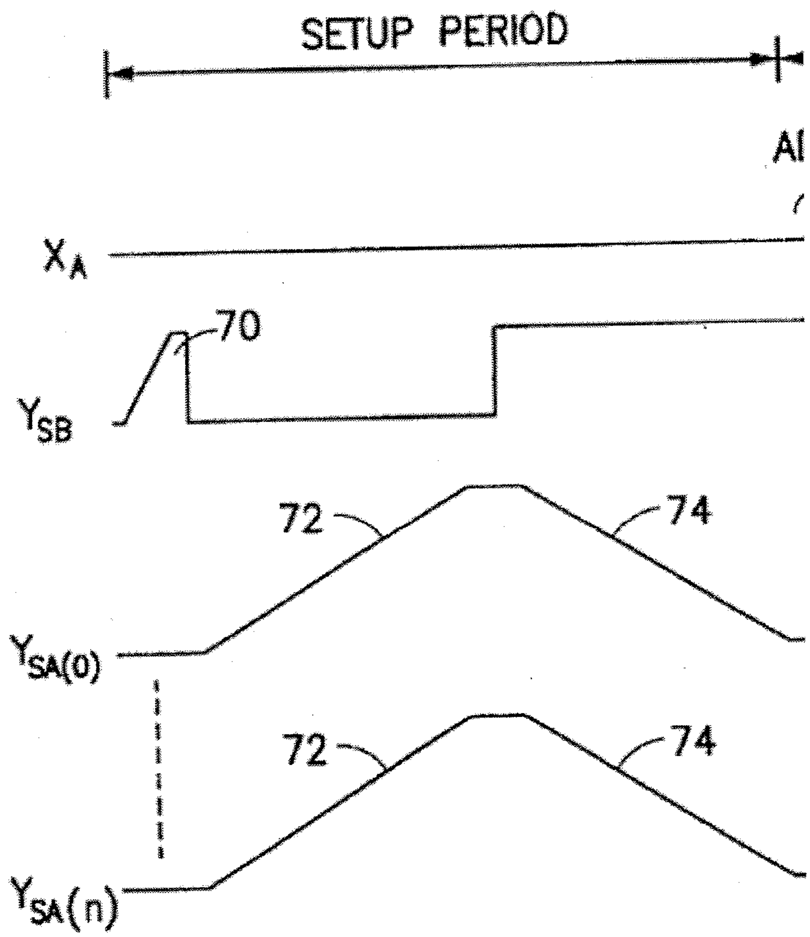
Applicant disclosed the Weber Article by Larry F. Weber entitled PLASMA DISPLAY DEVICE CHALLENGES (hereinafter "Weber Article") in previous Information Disclosure Statements submitted on January 31, 2007 and May 17, 2007, which were not considered in preparing the Office Action.

The Weber Article does not disclose "wherein the set-up pulse applied in the set-up step has a waveform that rises at an average voltage change rate of no greater than 6 V/μs and that starts to fall at a rate greater than the average voltage change rate at a time period of the rising."

The Weber Article provides that "An attractive solution that allows use of the weak discharge for setup was found by using ramp waveforms [5]." (Weber Article, Pg. 23) [5] refers

to Weber Patent (U.S. Patent 5,745,086, hereinafter "Weber Patent"), which has been made of record. (Weber Article, Pg. 27)

Weber Patent depicts in Figure 11:



Weber Patent states that:

> After the initial erase action, controller 50 operates a rise time control circuit 58 within Ysa sustainer module 54 which , in turn, applies a slowly rising ramp potential 72 to all sustain lines 28 (see Fig. 11). . . . At the end of the rising ramp of waveform 72, controller 50 then turns on a fall control circuit 60 which causes a slowly decreasing ramp voltage to be applied to all sustain lines 28.

(Col. 9, lns. 5 – 20). However, the slopes of 72 and 74 appear to be nearly identical.

As noted in *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, "A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would be lead away from the claimed invention." *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984); MPEP 2141.02.

In addition, the Weber Article states that:

> Figure 18 shows how a blue PDP sub-pixel behaves for differing ramp waveforms. The top half of Figure 18 shows the overlay of five different 300 volt sustain waveforms each having a differing ramp rise rate.

(Emphasis added) (Weber Article, Pg. 23)

The Weber Article further adds:

> From figure 18 it is obvious that there are two distinct discharge modes. The 1500 V/μs and the 15 V/μs ramps show a rapid pulsed type of light output. The 7.5 V/μs, the 3.75 V/μs and the 1.875 V/μs ramps show a lower peak intensity and a more steady state type of discharge that appears to have an amplitude proportional to the ramp rate.

(Weber Article, Pg. 24)

In contrast, in the present invention, set-up pulse rises at an average voltage change rate of no greater than 6 V/μs Furthermore, the set-up pulse "starts to fall at a rate greater than the average voltage change rate at a time period of the rising." The goals of the present invention is to have a short set-up period which makes it "possible to perform driving at a much higher speed" without write defects and to improve contrast to achieve superior image quality. (Pg. 20, lns. 8-19). By using a voltage that rises below 6 V/μs, a weak discharge is generated in an area where I-V characteristics are positive, and discharge takes place in an almost constant voltage mode so that the inside of the discharge cells is kept at a value Vf*, a little lower than the starting voltage Vf. This means that a negative wall charge corresponding to the potential difference (V-

Vf*) between the voltages V and Vf* can accumulate efficiently on the surface of the dielectric layer covering the scan electrodes 12a. If the average rate of voltage change α is set at 10 V/μs or more, the light emitted by the set-up pulse discharge is stronger and contrast drops markedly. If the average rate of voltage change α stays within this range, however, the light emitted by the set-up pulse discharge is much weaker than that emitted by the sustain discharge and contrast is almost totally unaffected. (Pg. 27, ln. 15 – Pg. 28, ln. 19). Thus, the benefits are realized by having the voltage rise below 6 V/μs Furthermore, by using a fall rate greater than the rise rate, the set-up pulse can be shortened to enable driving at a higher speed.

It is believed the present application is now allowable and an early notice of the same is requested.

If there are any questions with regards to this matter, the undersigned attorney can be contacted at the listed phone number.

Very truly yours,

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